FREQUENCY DIVISION/MULTIPLICATION WITH JITTER MINIMIZATION

ABSTRACT OF THE DISCLOSURE

A method and system described for producing frequency multiplication/division by any non-integer output signal frequency relative to a reference signal frequency of a Phase Lock-Loop (PLL), while simultaneously maintaining low jitter. In one embodiment, the invention increases the number of the available clock phases to M and then shifts the output clock phase by one, every K/M cycle. In one aspect of the present invention, this is accomplished by adding a multiplexer (MUX) to the output of the PLL to implement the phase shifting every K/M cycles. In another aspect, the MUX is placed in the feedback loop of the PLL. In one embodiment, a quantizer is used to drive the MUX.